Effect of Ionic Conductivity on Response Speed of SrTiO$_3$-Based All-Solid-State Electric-Double-Layer Transistor

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ABSTRACT: An all-solid-state electric-double-layer transistor (EDLT) with a Y-stabilized ZrO$_2$ (YSZ) proton conductor/SrTiO$_3$ (STO) single crystal has been fabricated to investigate ionic conductivity effect on the response speed, which should be a key parameter for development of next-generation EDLTs. The drain current exhibited a 4-order-of-magnitude increment by electrostatic carrier doping at the YSZ/STO interface due to ion migration, and the behavior strongly depended on the operation temperature. An Arrhenius-type plot of the ionic conductivity (σ_i) in the YSZ and t_c^{-1}, which is a current-rise time needed for charge accumulation at the YSZ/STO interface, shows a synchronized variation, indicating a proportional relationship between the two parameters. Analysis of the σ_i–t_c diagram shows that, in contrast to conventional EDLTs, the response speed should reach picosecond order at room temperature by using extreme miniaturization and superionic conductors. Furthermore, the diagram indicates that plenty of solid electrolytes, which have not been used due to the lack of criteria for evaluation, can be a candidate for all-solid-state EDLTs exceeding the carrier density of conventional EDLTs, even though the response speed becomes comparably lower than those of FETs.

KEYWORDS: electric-double-layer, all-solid-state, solid-state ionics, nanoionics, proton conductor
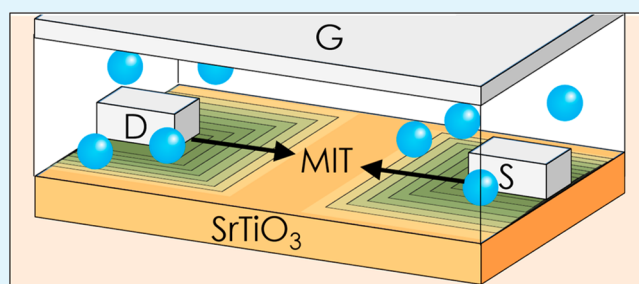
1. INTRODUCTION

Electrostatic carrier doping (ECD) of electronic materials is an attractive technique for exploring interesting physical properties due to its ability to easily control the electronic carrier density merely by adjusting the dc bias voltage and its freedom from the structural disorder inherent in chemical doping. Since the maximum carrier density obtained for conventional dielectric materials (e.g., Al$_2$O$_3$, SiO$_2$, Ta$_2$O$_5$) is on the order of 10^{13} cm^{-2}, the application of ECD has been limited to cases with low carrier densities.[1] Electric-double-layers (EDLs) of ionic-liquid electrolytes have been used to overcome this limitation, resulting in a much higher carrier density of 10^{14} cm^{-2}.[2−9] The interface metal−insulator transition (MIT), superconductivity, and magnetism resulting from the use of an EDL make this method potentially useful for discovering new material functions.[2−9]

While non-solid-state electrolytes, such as ionic-liquids, and ion-conducting gels enable high carrier density, compatibility with other electronic devices is problematic. The nonuse of liquids and gels is thus beneficial for practical applications. Accordingly, all-solid-state electric-double-layer transistors (EDLTs) using solid electrolytes are strongly desired.

While there are a variety of solid electrolytes available,[10] conducting ion species reported for all-solid-state EDLTs so far are limited to only proton and oxide ions which tend to show

comparably high conductivity.[11−17] One hindrance to development of solid electrolytes is the lack of criteria for evaluating the solid electrolytes suitable for use in EDLTs. Their ionic conductivity, σ_i, is a key parameter for the switching response as implied in the report for EDLTs containing an ionic-liquid and an ion-conducting gel.[4] This is a particularly important parameter for EDLTs using solid electrolytes, which usually exhibit a far lower σ_i (<10^{-5} Ω^{-1} cm^{-1}) than non-solid-state ones (>10^{-3} Ω^{-1} cm^{-1}) at room temperature.[10] In short, criteria of σ_i for evaluating available solid electrolytes are needed for further development of all-solid-state EDLTs.

In the present study, an all-solid-state EDLT using SrTiO$_3$ (STO) single crystal and a Y-stabilized ZrO$_2$ (YSZ) solid electrolyte was fabricated. While ionic conductivity of YSZ thin film is not so high (10^{-8} Ω^{-1} cm^{-1} at 523 K), it shows very unique V-shaped non-Arrhenius-type temperature dependence, which makes comparison of the conductivity and the other parameters much easier. Electrochemical analysis of its switching behavior was performed at various temperatures to investigate the EDL charging process. The ionic conductivity effect on EDLT performance and an availability of solid
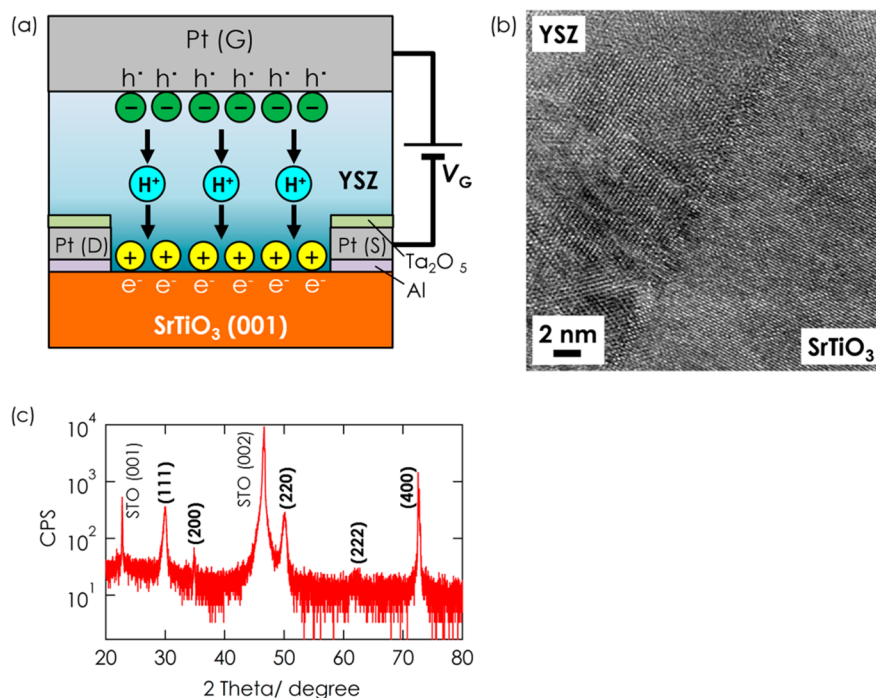
Figure 1. (a) Schematic illustration of STO-based EDLT using YSZ proton conductor and STO single crystal. Yellow and green circles represent positive and negative charges accumulated at interfaces due to proton migration. Light blue H^+ represents positive protons. (b) HR-TEM image of YSZ/STO interface. (c) XRD pattern of YSZ/STO.

electrolytes were discussed on the basis of a σ_i–t_c (current-rise time) diagram.

2. RESULTS AND DISCUSSION

2.1. Device Fabrication and Characterization. The all-solid-state EDLT, schematically shown in Figure 1a, was fabricated on an atomically flat (001) surface of undoped STO single crystal. A 700-nm-thick YSZ thin film was deposited by pulse laser deposition using a sintered 10% Y-doped ZrO_2 target pellet with 99.9% purity under a supply of pure oxygen gas at a fixed flow rate of 10 sccm to keep the oxygen pressure at 10 Pa. The substrate temperature was kept at 973 K during the deposition process. The high-resolution transmission electron microscope (HR-TEM) image of the YSZ/STO interface shown in Figure 1b reveals polycrystalline YSZ. The X-ray diffraction (XRD) pattern shown in Figure 1c reveals the cubic phase of ZrO_2 with low crystallinity. The source and drain were made of a 60-nm-thick platinum thin film. The gate electrode was made of a 150-nm-thick platinum thin film. These electrodes were deposited by RF sputtering with a shadow mask at RT before the YSZ thin film was deposited. The channel length and width were 75 and 50 μm, respectively. There were 10-nm-thick aluminum thin films inserted to eliminate Schottky barriers at the source/STO and drain/STO interfaces. There were 10 nm-thick tantalum oxide (Ta_2O_5) thin films inserted to prevent proton redox reaction at the Pt/YSZ interface. Electrochemical measurements were performed in air using a Keithley 4200-SCS parameter analyzer.

An Arrhenius-type plot of σ_i in the YSZ thin film measured by ac impedance spectroscopy using a Pt/YSZ/Pt two terminal cell is shown in Figure 2a. σ_i at various temperatures was calculated from a resistance for YSZ thin film (R) indicated in ac impedance spectra shown in Figure 2b. The V-shaped non-Arrhenius-type behavior, which is related to proton con-
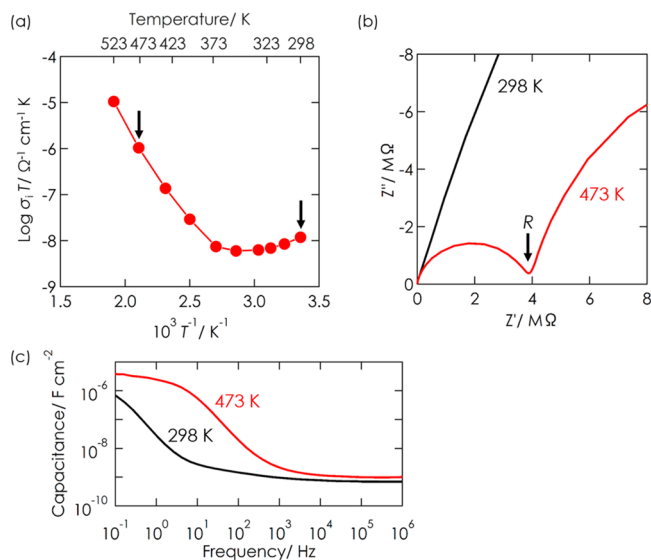
Figure 2. (a) Arrhenius-type plot of ionic conductivity, which was estimated from ac impedance spectroscopy. Black arrows indicate two temperature conditions (298 and 473 K) used for measurement of electrical conduction characteristics of EDLT for which results are shown in Figures 3 and 4. (b) Alternating current impedance spectra measured at 298 and 473 K. (c) Frequency dependence of capacitance measured at 298 and 473 K.

ductivity, was similar to previous reports.[18−21] Such low-temperature proton conductivity is known to arise from porosity.[22,23] Although the ion conduction mechanism is an important topic, the details will be discussed in a latter section (section 2.3). The electrical conduction characteristics of the EDLT were examined at two temperature conditions (298 and 473 K) indicated by black arrows in Figure 2a. Figure 2c shows the frequency dependence of capacitance at two temperature
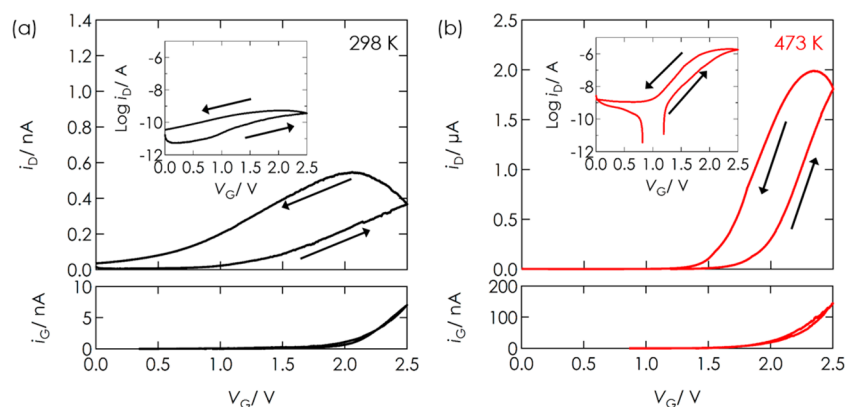
Figure 3. Electrical conduction characteristics of STO-based EDLT measured at 298 K (a) and 473 K (b) in air: i_D vs V_G (upper panel) and i_G vs V_G (lower panel). Sweeping rate of V_G was 4 mV/s. Insets show i_D vs V_D characteristic in log scale. Black arrows indicate V_G sweeping direction.

conditions. The capacitance at 298 K is much smaller than that at 473 K above 0.1 Hz, indicating very slow EDL charging kinetics at 298 K.

2.2. Electrical Conduction Characteristics of the EDLTs. The upper panels in Figure 3a,b show the electrical conduction characteristics (i_D vs V_G) for a constant V_D of 0.5 V at 298 K (part a) and 473 K (part b) in air of an STO-based EDLT gated by proton migration in YSZ. The i_D and V_G are the current through the drain and the voltage through the gate, respectively. The V_D is the voltage between the drain and source. In this study, only the V_G region above 0 V was examined in the same way with previous reports.[2,5,24] The EDLT exhibited very small increments in i_D from about 10 pA to about 550 pA, an order of magnitude difference at 298 K as shown in Figure 3a. In contrast, at 473 K, the EDLT exhibited steep increments in i_D from less than nanoampere order to microampere order, a 4-order-of-magnitude difference, for V_G above 1.2 V. This substantial difference between the two temperature conditions is attributed to the temperature dependence of σ_i in YSZ which is shown in Figure 2a. This will be discussed in detail in a later section on the basis of the temperature dependence of the EDLT response behavior.

Gate leakage current can affect the drain current when i_G is relatively large as observed in the V_G region above 2 V in Figure 3a. In such conditions, the effect of i_G should appear as a negative offset of i_D. It is because V_G being larger than V_D (=0.5 V) results in negative current from drain to gate electrode. Increase in i_D thus cannot be attributed to increase in gate leakage current. Furthermore, leakage current between drain and gate electrodes is far smaller than that between source and gate electrodes because the voltage between drain and gate electrodes ($=V_G - V_D$) is much smaller than the voltage between source and gate electrodes ($=V_G$). Accordingly, the effect on i_D should be very small.

The electrical conduction characteristics were accompanied by a considerable amount of hysteresis at both temperatures. This suggests that an electronic carrier was generated by the EDL at the YSZ/STO interface due to accumulation of ionic species with comparably slow kinetics, which is characteristic of ion migration-related phenomena.

The field-effect mobility of electron, μ, of the device at 473 K was estimated to be 0.62 cm^2/V s by applying

$$\mu = \frac{L}{WCV_D}\frac{\partial i_D}{\partial V_G} \tag{1}$$

to the i_D versus V_G characteristic, where L, W, and C are the channel length, channel width, and specific capacitance of the channel, respectively. A value of 4 μF cm^{-2}, measured with an ac impedance spectroscopy at 0.1 Hz, was used as the specific capacitance of the channel. The capacitance in the EDLT was less than half that of all-solid-state EDLTs using a Gd-doped CeO$_2$ (GDC) oxide ion conductor (14 μF cm^{-2}) and of ionic-liquid EDLTs (13 μF cm^{-2}).[5,16] The estimated μ is slightly better than that of the EDLT using GDC (0.55 cm^2/ Vs) and comparable to those (0.4 to 0.7 cm^2/(V s)) of other type field-emission-transistors (FETs) using STO single crystal.[25,26] In contrast to that at 473 K, the estimated μ at 298 K was unreasonably small value due to the extremely small variation in i_D. This indicates that a large potential drop occurred across the electrolyte layer due to the low σ_i and that the effective voltage applied to the EDL was reduced by the potential drop.

The lower panels in Figure 3a,b show the variation in i_G corresponding to the EDL charging current during V_G sweeping. In principle, the EDL charging current should be identical for 298 and 473 K because of the constant V_G sweeping rate. Furthermore, the increased i_G in the large V_G region was not completely relaxed to zero in constant V_G measurements, in contrast to i_G in the small V_G region. Accordingly, the substantial i_G increment at 473 K, particularly above a V_G of 2 V, indicates that there was a leakage current contribution at 473 K. This leakage current is attributed to an electrochemical reaction of protons at the YSZ/source and YSZ/drain interfaces. Even though the source and drain electrodes were covered by a 10-nm-thick Ta$_2$O$_5$ layer, as shown in Figure 1a, the narrow bare parts at the edge of the source and drain electrodes could have acted as a reaction field for the electrochemical reduction of protons, 2H$^+$ + 2e$^-$ → H$_2$. This reaction is comparably active on the surface of platinum. The bare parts of the electrodes thus caused an increase in the electrochemical reduction current. Furthermore, a slight amount of proton migration through the Ta$_2$O$_5$ layer, which is enhanced at an elevated temperature, to the source and drain electrodes may have increased the electrochemical reduction current.[27]

Figure 4 shows a plot of the i_D versus V_D characteristic at 473 K for various V_G values from 1.3 to 2.2 V. The lower panel is shown in a smaller current scale for small V_G values, and the upper panel is shown in a larger current scale for large V_G values. The i_D versus V_D characteristic in the lower panel reveals typical FET behavior with a transition from the linear i_D region to the saturation region. The linear region was slightly curved
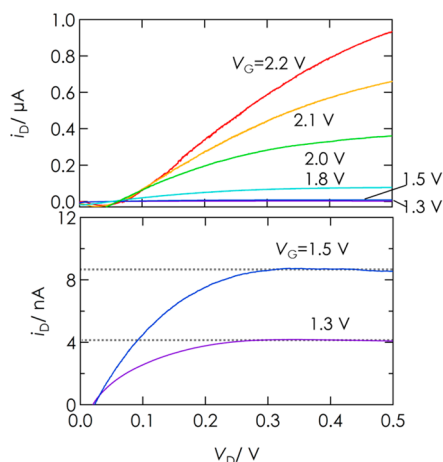
Figure 4. i_D vs V_D characteristic for various values of V_G (1.3, 1.5, 1.8, 2.0, 2.1, and 2.2 V). Lower panel has smaller current scale for small V_G values (1.3 and 1.5 V) with results for large V_G values omitted. Upper panel has larger current scale for large V_G values (1.8, 2.0, 2.1, and 2.2 V).

due to the slow kinetics of EDL charging at the YSZ/STO interface. The threshold voltage, V_{Th}, was estimated to be 1.2 V on the basis of the relationship, $V_G - V_{Th} = V_{D,sat}$, where $V_{D,sat}$ is V_D at the transition point from the linear i_D region to the saturation region (0.3 V at a V_G of 1.5 V).[28] The V_{Th} corresponds to the threshold voltage for MIT in STO, which

occurs at about 4.5×10^{17} to 2×10^{18} cm^{-3} of the carrier density.[29−32] The estimated V_{Th} agrees well with the electrical conduction characteristics shown in Figure 3b. The absence of a saturation region above a V_G of 2 V is reasonable because $V_{D,sat}$ ($=V_G - V_{Th} > 0.8$ V) is beyond the measurement range of V_D (from 0 to 0.5 V). Note that the value of V_{Th} includes errors due to the slow kinetics of the EDL charging process discussed in a later section.

2.3. Temperature Dependence of the EDLT Response Behavior. To investigate the relationship between σ_i and the EDL charging process in the EDLT, the temperature dependence of the EDLT response behavior was examined. The variation in i_D over time for a constant V_G of 2 V and a constant V_D of 0.5 V is shown in Figure 5a for various temperatures. The i_D rapidly increased to being on the order of several hundred nanoamperes several seconds to several tenths of a thousandth of a second after V_G application. The magnification of the current-rise part shown in the lower panel clearly reveals that the current-rise time, t_c, became exponentially longer as the measurement temperature was decreased from 523 to 298 K. Such behavior was also observed for an EDLT using GDC.[16] On the basis of the EDL mechanism, this change in t_c is attributed to the incubation time necessary for charge accumulation at the YSZ/STO interface and the resulting connection of a conductive layer between the source and drain electrodes.

This incubation time can be understood by considering the equivalent circuit of the EDL charging process shown in Figure
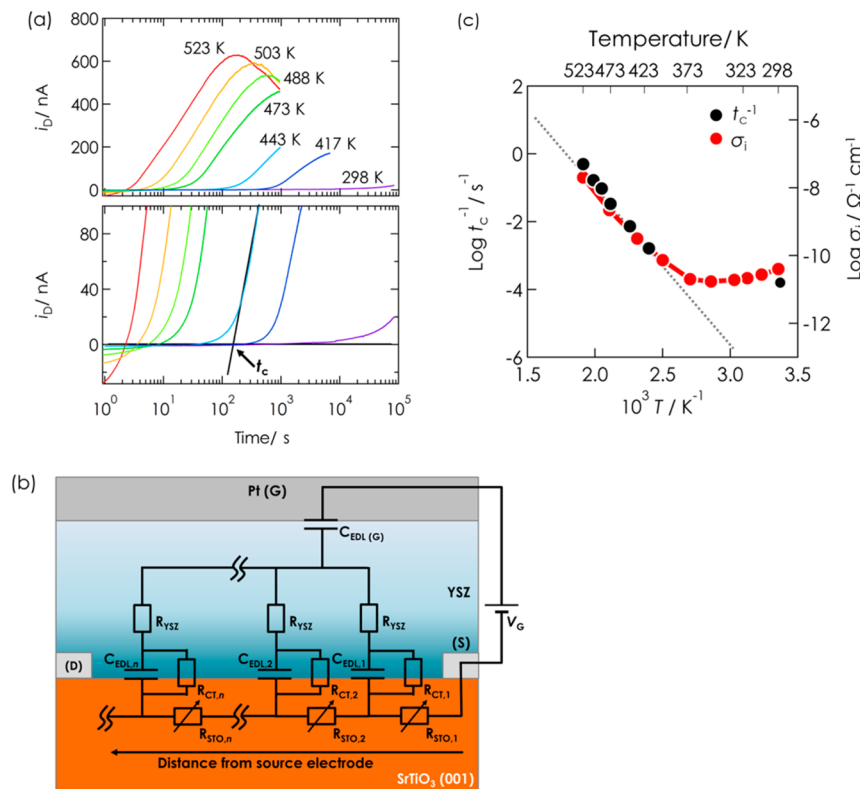
Figure 5. (a) Variation in i_D over time for constant V_G of 2 V, measured at various temperatures (523, 503, 488, 473, 443, 417, and 298 K). Prior to 2 V V_G application, V_G was kept at 0 V for 2000 s to eliminate the hysteresis effect of previous measurement. Lower panel shows magnification of the current-rise part. Current-rise time t_c is defined as cross point of approximated straight lines near the current-rise part. (b) Assumed equivalent circuit of EDL charging process. EDL charging propagates from both source and drain electrodes to the center of the channel. Only the source electrode side is depicted for simplification, but the effect of this on discussion is insignificant. (c) Arrhenius-type plot of t_c^{-1} (left axis) and σ_i (right axis). Red curve is additional curve for t_c^{-1}. Values on left and right axes represent 8 orders of magnitude.

5b, in which R_{STO}, R_{CT}, C_{EDL}, R_{YSZ}, and $C_{EDL(G)}$ are the resistance of STO at a certain position, the resistance of the charge transfer across the EDL, the EDL capacitance, the resistance of YSZ, and the EDL capacitance at the gate electrode/YSZ interface, respectively. R_{STO} is variable because the EDL charging at the position decreases the value due to the MIT. $C_{EDL(G)}$ is very large due to the gate electrode area being much larger than the channel area including the source and drain electrodes. This means that a potential drop at the interface is negligible.

When a gate voltage is applied, a large voltage is applied to the EDL in the vicinity of the source electrode (e.g., at $n = 1$), which is expressed by the parallel connection of $C_{EDL,1}$ and $R_{CT,1}$, resulting in EDL charging accompanied by a decrease in $R_{STO,1}$. In contrast, EDL charging does not occur at a position far from the source electrode (e.g., $n = k \gg 1$) due to the large potential drop in the serial connection of $R_{STO,n}$ [with n from 1 to k $(\sum_{n=1}^{k} R_{STO,n})$]. The MIT in the STO thus occurs only in the vicinity of the source electrode ($n = 1$) within a time period enough for EDL charging at the $n = 1$ position. After the EDL charging at the $n = 1$ position, however, EDL charging at the second nearest position (e.g., at $n = 2$) starts due to the decrease in $R_{STO,1}$ and the potential drop at the $n = 1$ position. This further extends the conductive region to the $n = 2$ position. Finally, the successive occurrence of EDL charging results in the connection of a conductive layer between the source and drain electrodes after a certain time period, that is, t_c (which is the total time needed for MIT at all positions in the current path).

Let us consider EDL charging only in the one circuit with $n = 1$. The accumulated charge at $C_{EDL,1}$, Q_1, is expressed as a function of the time (t) after application of V_G to the EDL ($n = 1$) is started, by the following equation under the condition that R_{CT} is far larger than R_{YSZ}:

$$Q_1(t) = C_{EDL,1}V\left(1 - \exp\left(\frac{-t}{R_{YSZ}C_{EDL,1}}\right)\right) \qquad (2)$$

Here V is the voltage effectively applied to the EDL. $C_{EDL,1}V$ equals the maximum charge (Q_m). Given the critical charge for MIT in STO as Q_c, eq 2′ is derived

$$Q(t') = Q_c = Q_m\left(1 - \exp\left(\frac{-t'}{R_{YSZ}C_{EDL,1}}\right)\right) \qquad (2')$$

where t' is the time needed for the MIT at the $n=1$ position. Equation 2′ is transformed into

$$t' = R_{YSZ}C_{EDL,1}\ln\left(1 - \frac{Q_c}{C_{EDL,1}V}\right) \qquad (2'')$$

Given the connection of a conductive layer by the successive occurrence of MIT at a total of kL positions, the relation

$$t_c = kLt' \qquad (3)$$

is obtained, where k and L are the specific number of virtual positions in the conductive channel and the channel length, respectively. kL thus corresponds to the virtual number of positions in the conductive channel. R_{YSZ} is replaced by T/σ_i, where T is the thickness of the YSZ layer (cm). Substituting t' into eq 3 by using eq 2″ gives

$$t_c = -\frac{kLC_{EDL}T}{\sigma_i}\ln\left(1 - \frac{Q_c}{C_{EDL}V}\right) \qquad (4)$$

The variation in t_c with respect to various parameters will be discussed using eq 4 in a later section. Given that Q_c, V, and C_{EDL} are independent of temperature, eq 4 can be regarded as $t_c\sigma_i = $ const. Accordingly, t_c^{-1} is proportional to σ_i. The critical carrier concentration for MIT in STO shows no significant temperature dependence from 4 K to RT.[29] Although the behavior above RT was not well-known, we assumed a temperature-independent Q_c based on an analogy. On the other hand, we do not have reliable evidence for the temperature-independent V and C_{EDL}. The assumption for V and C_{EDL} are thus rough. The calculation based on the assumptions, however, gives comparably good agreement with experimental results as shown below.

Figure 5c shows the variation in t_c^{-1} and σ_i for various temperature conditions from 298 to 523 K. The plot of the two parameters agrees with the master curve (shown in red). That is, eq 4 holds over the entire temperature range. Both t_c^{-1} and σ_i show Arrhenius-type behavior above 393 K with an activation energy of 1.01 eV (gray dotted line). On the other hand, non-Arrhenius type behavior was observed for both parameters below 393 K. The behavior is similar to the V-shaped non-Arrhenius-type curve shown in Figure 2a.[15] The comparably large activation energy of 1.01 eV above 393 K indicates a predominant contribution from oxide ion conduction to the total ionic conductivity.[15] The conductivity of 10^{-8} Ω^{-1} cm^{-1} at 523 K agrees well with that of YSZ pellets, supporting the validity of the assignment.[33] It is interesting to note that the unique V-shape temperature dependence of σ_i in YSZ agrees well with the behavior of t_c^{-1}.

While there has been a debate about electrochemical carrier doping in STO-based EDLT featured by complete suppression of metallization in the presence of oxygen gas,[24] no indication of the suppression was observed in this study, supporting electrostatic carrier doping in the EDLT. Furthermore, given electrochemical reduction of STO for the carrier doping mechanism, the response speed should depend on reaction activity of electrochemical reduction of STO. In contrast, the temperature dependence of t_c^{-1} agreed with the unique V-shape temperature dependence of σ_i in YSZ as shown in Figure 5c. This relationship is well-explained by the EDL charging model discussed above. The result also supports electrostatic carrier doping. We thus deem that electrostatic carrier doping is a reasonable explanation for the carrier doping behavior in the EDLT. Reaction activity for electrochemical reaction is strongly dependent on electrodes, electrolytes, and the combination as observed in wide spectrum of electrochemical systems (e.g., batteries, sensors). The difference between this work and the previous report[24] can be attributed to the difference in reaction activity for electrochemical reduction of STO between the devices. Further effort is needed for the clarification.

Related to the present work, a transfer of oxygen vacancy from one oxide to the other was recently reported.[34] While the issue is important for clarifying details of the mechanism, we would like to leave it for future work.

2.4. σ_i–t_c Diagram for an STO-Based EDLT. The value of k for the EDLT calculated using the fitting in Figure 5c was 1.55×10^6 cm^{-1}. The σ_i–t_c diagram for an STO-based EDLT can be drawn by applying the value of k to eq 4. A diagram for various C_{EDL}, T, and L is shown in Figure 6. As expected from eq 4, all of the t_c plots are inversely proportional to σ_i. This
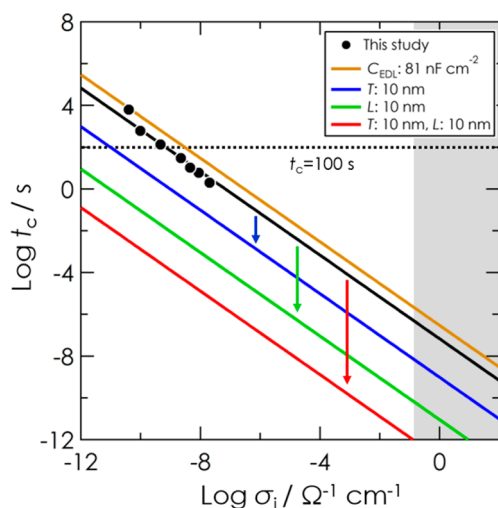
Figure 6. $\sigma_i - t_c$ diagram for various parameters. Black circles represent experimental results plotted in Figure 5c. The black line is an additional line for the experimental results calculated using 4 μF cm^{-2} for C_{EDL}, 700 nm for T, and 75 μm for L. The yellow-brown line represents the calculation results when only C_{EDL} was changed (to 81 nF cm^{-2}). The blue line represents the calculation results when only T was changed (to 10 nm). The green line represents the calculation results when only L was changed (to 10 nm). The red line represents the calculation result when both T and L were changed (to 10 nm). V_G of 2 V was assumed for all calculations. The gray region indicates where solid electrolytes are not present at room temperature.

dependence agrees well with the experimental results, which are also plotted. An increase in C_{EDL} from 81 nF cm^{-2} (shown by yellow brown line) to 100 μF cm^{-2} (shown by black line), more than 4 orders of magnitude, causes a very slight decrease in t_c (77% shorter than the t_c for 81 nF cm^{-2}). The complete saturation of the variation above 1 μF cm^{-2} indicates that the value of C_{EDL}, which is usually above 1 μF cm^{-2}, has almost no effect on t_c. On the other hand, a decrease in T and L (blue and green lines, respectively) causes a decrease in t_c by several orders of magnitude. The result of calculation with value of 10 nm for both T and L, values presumably achievable by using lithography-based miniaturization, is shown by the red line. The cross point with a log σ_i of -1 indicates that extremely small EDLT devices using (solid-state) superionic conductors with an extremely high σ_i (exceeding 10^{-1} Ω^{-1} cm^{-1}), e.g., RbAg$_4$I$_5$, should have a response speed on the order of a picosecond, in contrast to conventional all-solid-state EDLTs with best operating frequency of 2 Hz.[11−17]

Let us discuss the physical meaning of k in the present switching model. The reciprocal of k, k^{-1}, has a dimension of length. The length corresponds to the length of the one unit circuit (e.g., with $n = 1$) discussed in section 2.3. The value of k^{-1} in this study was calculated to be 6.5 nm. This can be interpreted that the conductive layer extends 6.5 nm after each EDL charging, which needs t' to finish. Since the conductive layer actually extends from both the source and drain electrodes, the conductive layer extends half of 6.5 nm, 3.25 nm from both electrodes. Given very long k^{-1}, e.g., $L = k^{-1}$, the switching process is approximated by MIT by single EDL charging because t' is equal to t_c. On the contrary, the switching character changes to the successive one as k^{-1} becomes short. In an extreme case with $k^{-1} = 0$, connection of the conductive layer is not achieved anymore. Since the value of k^{-1} is related

to resistivity of the channel in OFF state, it may be influenced by the quality of the solid electrolyte/channel interface.

3. CONCLUSION

An all-solid-state EDLT using STO single crystal and YSZ thin film was fabricated, and the ionic conductivity effect on the i_D response was investigated. While the ionic gating on the EDLT resulted in a large resistance change (4 orders of magnitude) at 473 K, the resistance change was very small at 298 K (about an order of magnitude). The temperature dependence of the i_D response of the EDLT was analyzed, and a $\sigma_i - t_c$ diagram was created. The values in this diagram can be used as evaluation criteria in the development of all-solid-state EDLTs containing various electrolytes although they depend on the channel material to some extent. The development of all-solid-state EDLTs should enable application of EDLTs, which has been limited to fundamental research due to the poor compatibility of liquids with electronic devices, to various practical applications. The result presented here indicates that a variety of solid electrolytes and conducting ionic species (e.g., Ag$^+$, Cu$^+$, Na$^+$, Li$^+$), which have not been used for conventional all-solid-state EDLTs, can be usable. It also indicates that extremely high-performance EDLTs with high speed can be achieved by using extreme miniaturization and superionic conductors.

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